REMARKS:

This paper is herewith filed in response to the Examiner's Office Action mailed on January 7, 2008 for the above-captioned U.S. Patent Application. This office action is a rejection of claims 1-2, 4-9, 11-12, 14-19, 21-22, 24-29, and 32-33 of the application.

More specifically, the Examiner has rejected claims 1-2, 4, 8-9, 11-12, 14, 18-19, 21-22, 24, 28-29, and 32-33 under 35 USC 103(a) as being unpatentable over Horowitz (US7,142,612) in view of NG (US6,737,995); rejected claims 5-7, 15-17, and 25-27 under 35 USC 103(a) as being unpatentable Horowitz in view of NG and further in view of Huang (US5,798,535); and objected to claims 3, 10, 13, 20, 23, 30-31, and 34 as being dependent upon a rejected base claim, but allowable if rewritten in independent form. The Applicants thank the Examiner for the indication of allowance and respectfully traverse the rejections.

Claims 1, 3, 11-20, 23, and 34 have been amended for mere formality. Support can be found at least in the title, page 9 in line 1, and the abstract. No new matter is added.

Regarding the rejection of claim 1 under 35 USC 103(a) the Applicants respectfully disagree with the Examiner.

The Applicants note that in the rejection of claim 1 the Examiner states:

> "[Horowitz] does not teach a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods. However, Ng discloses a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods (col. 3 lines 32-40 and col. 4 lines 46-52). Therefore, taking the combined teaching of Ng and Horowitz as a whole would have been rendered obvious to one skilled in the art to modify Horowitz to utilize a data boundary to the receiver for the benefit of determining an offset based on consecutive data bits periods," (emphasis added).

The Applicants note that NG relates to a method of determining a slice level setting for detecting a high and low level of an incoming data stream in order to reduce signal noise.

NG discloses:

> "The receiver also includes a loop 24 to adjust the slice level at which the incoming data signals are sampled. The slice level adjustment loop 24 includes the offset detector circuitry and circuitry 26 to adjust the slice level," (col. 3, lines 23-26).

Further, the Applicants note that as cited NG discloses:

> "The circuitry 16 is configured to sample data during each data bit period and to sample the signal in the transition period between each pair of consecutive data periods. Referring, for example, to FIG. 2A, the circuitry 16 would sample the incoming data signal during a first period representing a first data bit period A and during a second period representing the next data bit period B. The circuitry 16 also samples a signal in the transition period T that occurs between the two consecutive data bit periods A and B," (emphasis added), (col. 3, lines 32-40); and
>
> "The state of the transition bit during a transition from a logical "1" to a logical "0" or vice-versa serves as the basis for either incrementing or decrementing the slice level adjustment signal provided to the summer 28. The offset may be measured based on the three signals sampled, respectively, during two consecutive data bit periods (A and B) and the intervening transition bit period (T)," (emphasis added), (col. 4, lines 46-52).

The Applicants note that the Examiner is apparently equating sampling two consecutive data bit periods (A and B) and an intervening transition bit period (T) in NG with "indicating a data boundary to the receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods," as in claim 1. The Applicants fail to see any relation between **sampling** the signals in NG and indicating a data boundary by **holding** a signal bus at the same level for two consecutive periods.

NG discloses:

> "Therefore, if values of the sampled signals [A, T, B] are consecutively [1, 1, 1] for a predetermined number of times, the circuitry 16 generates a slice level control signal to increase the signal fed back to the summer 28," (emphasis added), (col. 5, lines 10-13); and
>
> "In situations where that is not the case, such as when the values of [A, T, B] are [1, 0, 1] or [0, 1, 0], it is assumed that an error occurred, and the circuitry 16 does not generate a slice level control signal to decrease or increase the signal fed back to the summer 28," (emphasis added), (col. 5, lines 18-22).

Here it can be seen that NG clearly evaluates a similar amplitude level of the consecutive data bit periods A and B differently depending on a value of the transition bit period T. As stated above if the values for A, T, B are 1, 1, and 1 then NG generates a slice control signal. However, if the consecutive data bit periods A and B are an equal value, such as 1 and 1, but the transition bit period T is an opposite value, such as 0, then NG assumes that an error has occurred. The Applicants submit that the operation of NG is clearly distinguishable from claim 1.

The Applicants contend that NG can not be seen to relate to indicating a data boundary to a receiver by holding one of the multi-level signal buses at the same level for at least two consecutive bit periods as in claim 1.

Further, NG discloses:

> "The slice level adjustment loop 24 causes the slice level to converge to a level where the probability of detecting a logical "1" for the transition bit is substantially equal to the probability of detecting a logical "0" for the transition bit. Even if the rise and fall times are not the same, the loop 24 can help reduce jitter," (emphasis added), (col. 3, line 64 to col. 4, line 3).

It can be seen that here NG is concerned with the probability of detecting merely a 1 or a 0. Moreover, the Applicants submit that NG is merely seen to relate to sampling signal values and adjusting the slice level such that the data periods A and B, and the transition period T in NG are most clearly detectable to indicate **the logical value of either a 0 or 1**. Clearly, for at least this reason NG can not be seen to relate to **multi-level analog signals** comprising **more than two analog amplitude levels** as in claim 1.

Furthermore, for at least the reasons stated the Applicants contend that the combination of Horowitz and NG would at least require a redesign of both the references which is against the rules regarding an obviousness rejection.

The Applicants submit that for at least the reasons stated a person skilled in the art would not be motivated to combine Horowitz and NG. Moreover, the Applicants contend that even if Horowitz and NG were combined, though not agreed to as proper, the combination would still not disclose or suggest claim 1.

Additionally, the Applicants submit that Huang can not be seen to address a shortfall of NG as stated above.

Further, for at least the reason that independent claims 11, 21, and 32 recite features similar to claim 1 as stated above, the Applicants contend that for at least the reasons stated the references cited can not be seen to disclose or suggest all claims 1, 11, 21, and 32.

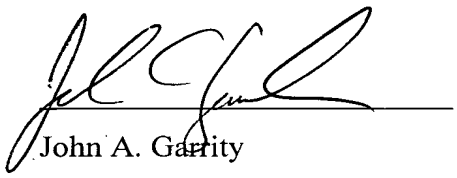
Further, for at least the reason that claims 2, 4, and 8-9; claims 12, 14, and 18-19; claims 22, 24, 28-29, and 33; depend from claims 1, 11, 12, and 32, respectively, the references cited are not seen to disclose or suggest these claims.

Furthermore, the Applicants note that although the arguments presented have not addressed all the rejections in the Office Action the Applicants do not acquiesce to these rejections.

Based on the above explanations and arguments, it is clear that the references cited cannot be seen to disclose or suggest claims 1-2, 4, 8-9, 11-12, 14, 18-19, 21-22, 24, 28-29, and 32-33. The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-34 and to allow all of the pending claims 1-2, 4, 8-9, 11-12, 14, 18-19, 21-22, 24, 28-29, and 32-33 as now presented for examination.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted:



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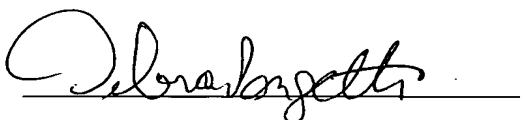
April 7, 2008



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